DS1624 2-Wire Communication SDA Hold Time Clarification

The 2-Wire timing specification of the DS1624 differs from that of I2C. This application note details the difference. SDA is not held internally by the DS1624. It is the bus master's responsibility to hold SDA until after the falling edge of SCL is completed.

Introduction

This application note details the difference between DS1624 communication timing and the I^2C™ specification. Under I^2C, the SCL and SDA lines are allowed to transition simultaneously because SDA is delayed internally by the slave device for at least 300ns. The DS1624 does not delay the SDA signal with respect to SCL therefore SDA must be held in the proper logic state by the bus master until SCL has fully transitioned to logic low to prevent false generation of START or STOP operations.

Proper Timing

The DS1624's SDA line does not have an internal delay relative to SCL. For this reason the SDA logic level must be held external to the DS1624 until SCL has transitioned to logic low when writing data; otherwise a start or stop condition may be recognized instead. When writing a logic "1" on the 2-wire bus, SCL must reach the guaranteed logic low threshold V_{IL} (0.3 x VDD maximum) before SDA transitions below the guaranteed logic high threshold V_{IH} (0.7 x VDD minimum). When writing a logic "0", SCL must reach V_{IL} before SDA transitions above V_{IL}. When generating a START condition, SDA must reach V_{IL} before SCL transitions below V_{IH}. When generating a STOP condition, SDA must reach V_{IH} before SCL transitions below V_{IH}. Both V_{IL} and V_{IH} levels are production tested on each device. This guarantees proper operation using this timing over the full voltage and temperature ranges including device fabrication tolerances.

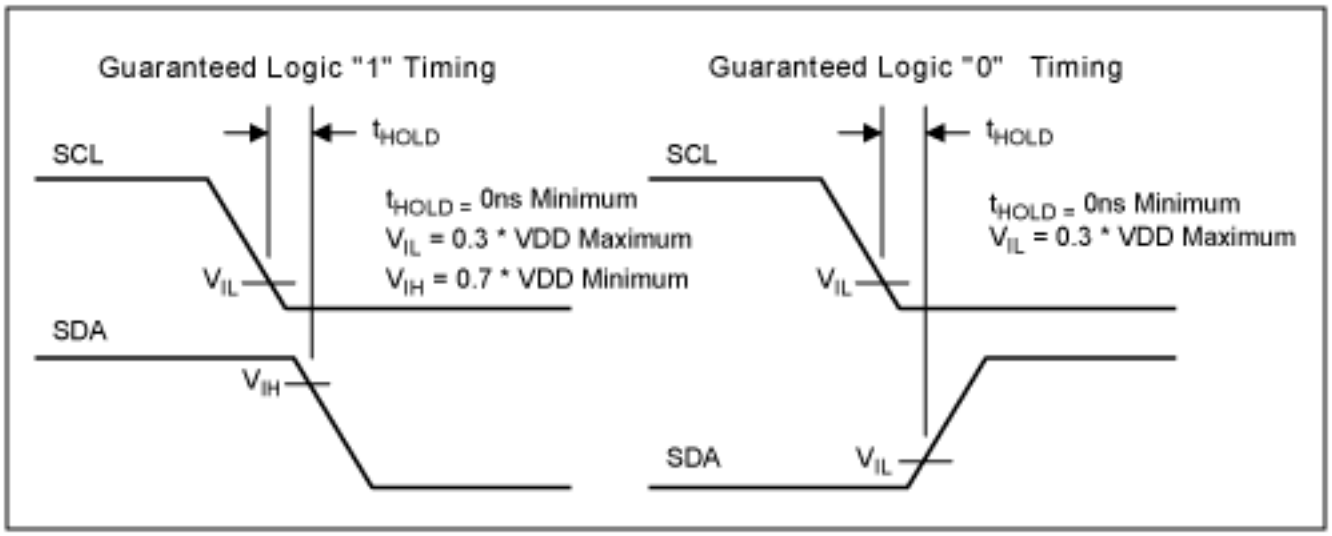

Figure 1.

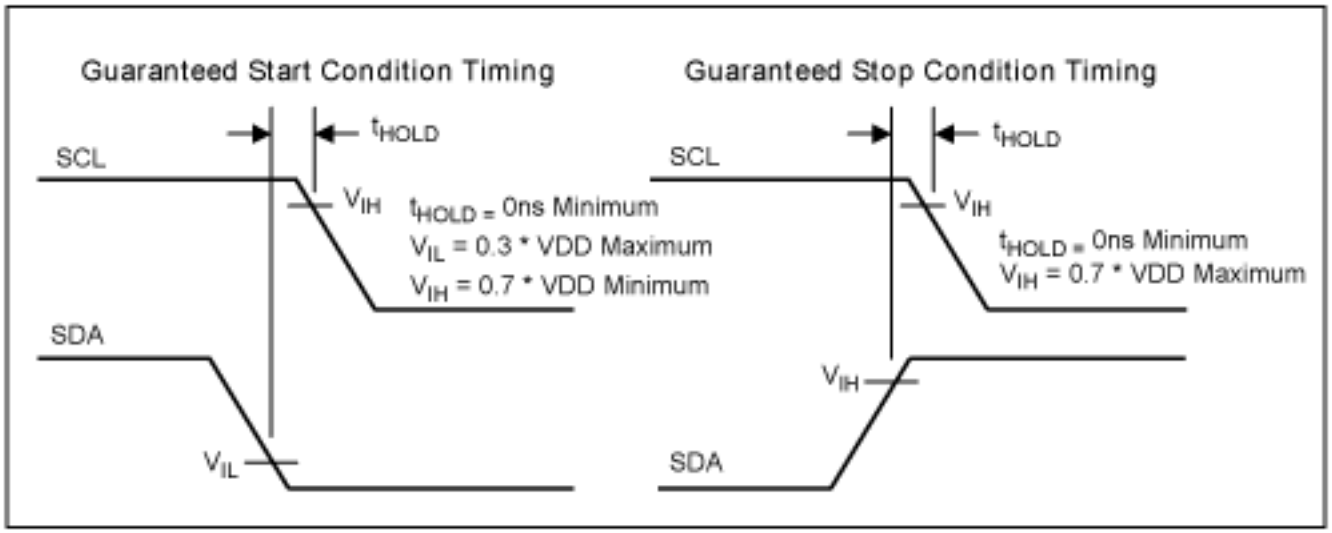

Figure 2.

Summary

There is a difference between the DS1624 timing and I²C specifications. The DS1624 does not internally delay SDA with respect to SCL. The system host is therefore required to maintain SDA during the falling edge of SCL to prevent logic '1's from being interpreted as START conditions and logic '0's from being interpreted as STOP conditions.

More Information

DS1624: QuickView -- Full (PDF) Data Sheet -- Free Samples